**Vertical high-voltage GaN pin diodes on Si**

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GaN-based devices are excellent candidates for high-power switching applications. Currently, both vertical and lateral devices are being considered. GaN vertical devices have attracted increased attention recently, due to their high breakdown voltage (*BV*) and current capability for a given chip size, and superior thermal performance [1]. Record *BV* *vs* specific on-resistance (*R*on) performance have been demonstrated in GaN vertical transistors and diodes recently. However, current GaN vertical devices suffer from the need for expensive GaN substrates, which has become a main obstacle for their commercialization.

In 2014, we demonstrated the first GaN vertical devices on low-cost Si substrates with a *BV* of 300 V and *R*on of 10 mΩ·cm2 [2-3]. Recently, fully-vertical GaN-on-Si diodes were also presented by different technologies [4-5], with a *BV* of 288-350 V and *R*on of 3.3-7.4 mΩ·cm2. Despite these promising results, the *R*on and *BV* still need improvement to be competitive.

In this work, we demonstrate quasi- and fully-vertical GaN-on-Si pn diodes with record performance. High-quality GaN epi-layers as thick as ~3.7 µm were successfully grown on 2-inch Si substrate and ~3 µm transition layers [6]. Due to the limited total thickness of the GaN epitaxy on Si, the optimization of the thickness and doping in each GaN layer is the key to achieve superior *BV*~*R*on trade-off: (a) The n--GaN was lightly carbon-doped to compensate the non-intentional-doping, which enabled a low donor concentration (*N*D) ~1×1016 cm-3. (b) The n+-GaN is highly-doped with *N*D>1020 cm-3. According to 2-D TCAD simulation, this highly doped n+-GaN allows a higher current density and a much more spread current distribution in the drift region, and therefore lowers the *R*on of quasi-vertical pn diodes.

Our quasi-vertical GaN-on-Si pn diodes were demonstrated utilizing an optimized deep etching process and advanced edge termination technologies. The fully-vertical diodes were fabricated by using a layer transfer technology: the original wafer was flipped over and bonded to another Si substrate, with the original Si substrate and transition layers removed afterwards.

A *R*on of 0.8-1 mΩ·cm2, a *BV* over 500 V and a high forward current (~kA/cm2) were demonstrated for quasi- and fully-vertical diodes. The demonstrated forward current density is comparable to the state-of-the-art performance of GaN-on-GaN vertical diodes. Excellent *R*on and *BV* performance up to 300 oC was also obtained. A small reverse recovery time of 50 ns was demonstrated under switching conditions for both diodes.

With a record Baliga’s figure of merit for GaN-on-Si vertical pn diodes (over 0.32 GW/cm2), the performance shows the great potential of cost-effective GaN-on-Si vertical devices for future power applications.

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Reference: [1] Y. Zhang *et al.*, *IEEE Trans. Electron Devices*, vol. 60, no. 7, pp. 2224–2230, Jul. 2013. [2] Y. Zhang *et al.*,” *IEEE Electron Device Lett.*, vol. 35, no. 6, pp. 618–620, Jun. 2014. [3] Y. Zhang *et al*., *IEEE Trans. Electron Devices*, vol. 62, no. 7, pp. 2155–2161, Jul. 2015. [4] X. Zou *et al*., *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 636–639, May 2016. [5] S. Mase *et al*., Appl. Phys. Expr., vol. 9, no. 111005, Oct. 2016. [6] A. Dadgar, *Phys. Status Solidi B*, vol. 252, no. 5, pp. 1063–1068, May 2015.

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Fig. 3.Schematic cross sections of the main fabrication steps for fully-vertical GaN-on-Si pn diodes. The fully-vertical GaN-on-Si pn diodes were fabricated by using a layer transfer technology: the original GaN-on-Si wafer was flipped over and bonded to another (100) Si substrate, and the original (111) Si substrate and transition layers were removed.

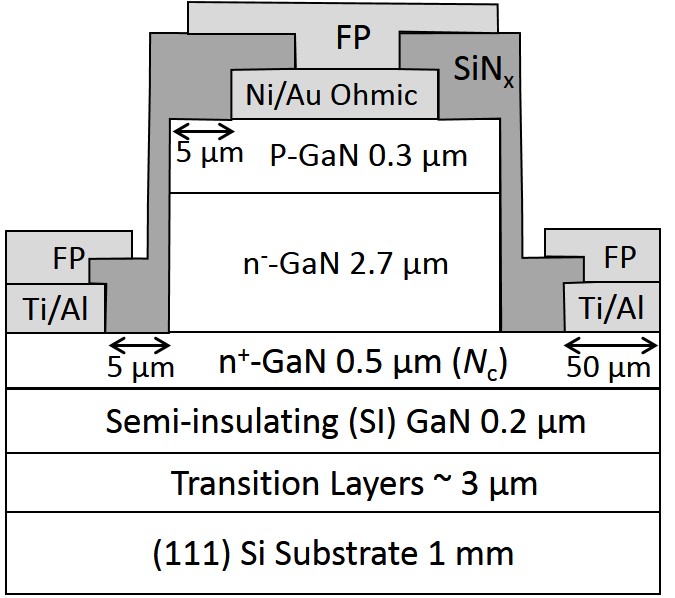


Fig. 1. Schematic cross sections of quasi-vertical GaN-on-Si pn diodes with passivation and field plate structures.

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Fig. 4. (a) Forward I-V and differential *R*on characteristics and (b) reverse I-V characteristics for the quasi- and fully-vertical GaN-on-Si pn diodes. (c) Forward I-V and differential *R*on characteristics and (b) reverse I-V characteristics of the quasi-vertical GaN-on-Si pn diodes at 25-300 oC. Similar high-temperature forward and reverse characteristics was observed for the fully-vertical pn diodes.

Fig. 5. *R*on *v.s.* *BV* of GaN-on-Si vertical diodes demonstrated in this work and the ones in previous reports for GaN vertical diodes. The forward current density is extracted at the bias for differential *R*on extraction.

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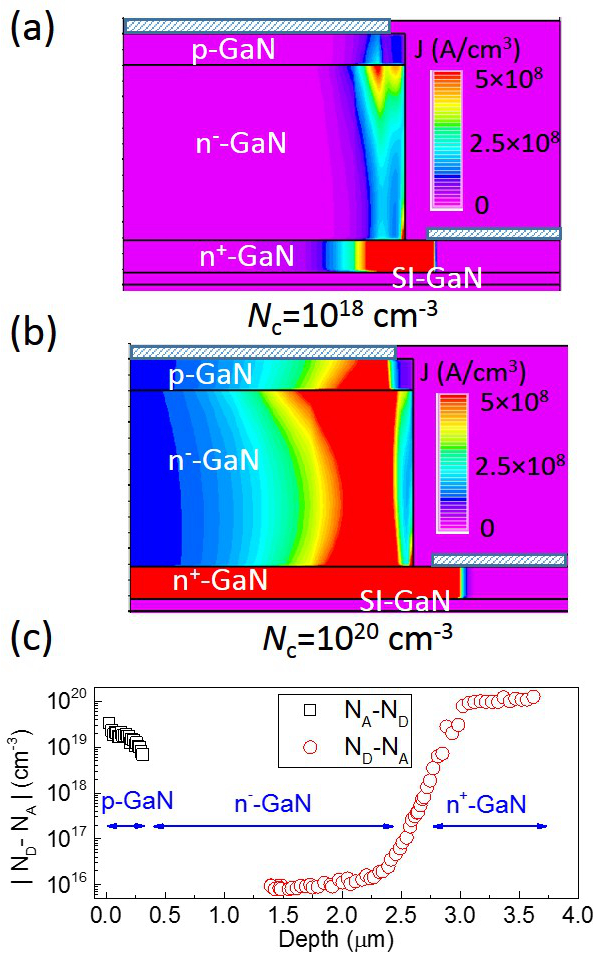


Fig. 2. (a) (b) Simulated forward current density distribution in quasi-vertical GaN-on-Si diodes with different doping levels in n+-GaN. (c) Net donor/acceptor concentration profile in the grown wafer, revealed by the electrochemical C-V measurement.